Improvement of Shipped Product Quality Level for Logic VLSIs Based on Semiconductor Layout

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OUTLINE

- Background
- Critical Area Analysis
- Weighted Fault Coverage
- SPQL for Benchmark Circuits
- Experimental Results from Renesas
- Steiner Tree and Critical Area

Brief History of PRDCs/PRFTSs

1989 Chongqing, China
1991 Kawasaki, Japan
1993 Melbourne, Australia
1995 Santa Barbara, CA
1997 New Port Beach, CA
1999 Hong Kong, China
2000 Los Angeles, CA
2001 Seoul, Korea
2002 Tsukuba, Japan 2004
Papeete, Tahiti

2005 Changsha, China
2006 Reverside, CA
2007 Melbourne, Australia
2008 Taipei, Taiwan
2009 Shanghai, China
2010 Tokyo , Japan
2011 Pasadena, CA
2012 Niigata, Japan
2013 Vancouver
2014 Singapole

2015 Zhangjiajie, Hunan, China
2017 Christ Church, New Zealand